ChipDesign B.V.B.A.:
RF IC Design Services & Antenna/MMIC Turn-Key Solutions

Koen Van Caekenberghe, Ph.D.
ChipDesign B.V.B.A.
E-Mail: info@chipdesign.be
Cell: +32484836572

ChipDesign B.V.B.A.

- ChipDesign B.V.B.A. is a private LLC according to Belgian law with VAT registration number: BE0501.767.340, founded in 2012. ChipDesign is located at Kapellelaan 302, 1860 Meise, Belgium.
- ChipDesign offers:
  - Services & turn-key solutions
    - ASIC design services
    - Device and process modeling services
    - Turn-key solutions
  - Open-source software
    - NF2FF
    - rfMaxima
    - Verilog-A large-signal RF MEMS model library

ChipDesign's RF IC Design Services

- ChipDesign offers front-to-back mixed-signal / RFIC design services in triple-well bulk and twin-well PD- and FD-SOI/SOS CMOS processes, covering ASIC specification, design, layout, functional verification, packaging and characterization:
  - ASIC specification: performance versus power trade-off and partitioning across building blocks (Mathworks MATLAB & Simulink, Verilog-AMS, wxMaxima)
  - ASIC design:
    - Analog/RF: passive (antenna matching tuner, attenuator, (TTD) phase shifter, SPNT switch, transformer) and active (image-reject mixer, multiplier, LNA, PA, VCO) design. Analysis of non-linear circuits (HB, and (Q)PSS solvers) (Agilent GoldenGate, Cadence Spectre/RF, interested in Mentor Graphics Eldo and Synopsys HSPICE).
    - Digital: design (Verilog, VHDL) and synthesis (Cadence RTL Compiler and Synopsys Design Compiler). Integration of serial I/O interfaces (I^2C, LVDS. RFFE, SPI) in ASICs.
    - EM: differential equation methods (FDTD, FEM), integral equation methods (TDIE, MoM/MLFMM). Interested in domain decomposition methods.
    - Mixed-signal: DAC (charge sharing, current steering), DDS, and PLL (PFD/CP, programmable divider, sigma/delta modulator) design. Interested in ADC and ADPLL design (BDA AFS, Cadence UltraSim).
    - Power management: AC-DC (voltage multiplier) and DC-DC (buck, boost, Dickson charge pump) converters, linear regulators (LDO, series), and voltage references (band gap).

ChipDesign's RF IC Design Services

- Front-to-back mixed-signal / RF IC design services (continued):
  - ASIC layout verification using DRC/LVS, parasitic extraction (Cadence Assura, Mentor Graphics Calibre), and EM simulation (Agilent Momentum, Ansys HFSS, CST Microwave Studio, Integrand EMX, Sonnet). IC yield optimization using foundry-supplied PCM data-based Monte Carlo and process corners simulation of extracted views.
  - RF IC floor planning (ESD protection, micro-bumps / pad ring, RF grounding) and RF IC packaging (DVN/QFN, WLCSP) and signal integrity analysis of PCB designs.
  - Mixed-signal ASIC functional verification using Verilog-AMS and digital ASIC/FPGA functional verification using SystemVerilog and UVM (Cadence Incisive).
  - On-wafer ASIC characterization, incl. large-signal S-parameter, noise (NF, phase noise), and non-linear measurements (ACPR, CSO, CTB, IP3, P1dB, XMOD). ASIC debugging (FIB).
  - Electronic design automation using Agilent AEL, Ansys VBScript, Cadence OCEAN, Python, ROD and SKILL, and Tcl.
- ChipDesign provides device and process modeling (Silvaco TCAD, Verilog-A) and characterization (Agilent IC-CAP) services:
  - III-V compound semiconductor (D/E-mode GaAs pHEMT, interested in GaN HEMT and InSb DHBT) and silicon-based (SiGe:C HBT) semiconductor devices
  - Capacitive MEMS and piezoelectric devices (accelerometers, gyroscopes, inertial measurement units, microphones, resonators (incl. quartz crystal, SAW and BAW resonators), switches)

ChipDesign's Antenna/MMIC Turn-Key Solutions

- ChipDesign also offers turn-key RF solutions to customers. Examples include:
  - Antennas and antenna arrays
  - ASIC packages (BGA/LGA, DVN/QFN, SOT, WLCSP)
  - Class A through S PAs based on GaN or LDMOS transistors, incl. tunable matching networks for optimal load-pulling, as well as Doherty, EER (Kahn), ET and outphasing SSPA transmitters.
  - RF and mixed-signal PCB design and layout
  - PDK development

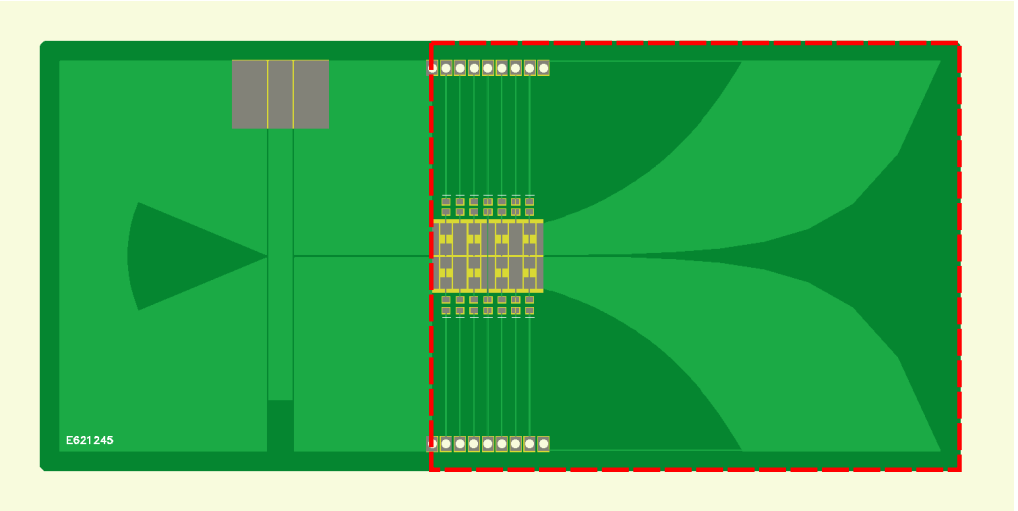


Figure 1: A differential RF MEMS reflectarray brick with 3:1 bandwidth (slotline RF MEMS TTD phase shifter DETSA) for a wideband brick assembled reflectarray for mobile backhaul applications.

ChipDesign's Open-Source Software

ChipDesign uses and contributes to open-source EDA software in order to lower costs:

- NF2FF: *NF2FF* is a planar near-field to far-field transformation script, written in MATLAB, for antenna measurements. Near field (NF) ranges offer a convenient alternative to compact antenna test ranges (CATR) and anechoic far field ranges for the measurement of phased arrays. NF sites allow for hologram analysis, low sidelobes characterization, and do not require a rotating pedestal capable of bearing the weight of the phased array. The primary objective of the NF2FF sourceforge project is to provide the phased array community with an open-source MATLAB alternative to proprietary NF measurement software. The code features planar near field to far field transforms with rectangular waveguide probe correction. The secondary objective of the project is to implement various functions for phased array hologram analysis. Phased array holograms allow for faulty element localization and for measurement of active element amplitude and phase excitation, in transmit (Tx) as well as in receive (Rx) mode, which allows for insight in the difference between achieved and desired Tx and Rx array factor. In addition, active element Tx and Rx root mean square (RMS) amplitude and phase error can be measured which allows for insight in beam pointing error and side lobe level increase, and gain reduction, while scanning. http://nf2ff.sourceforge.net
- rfMaxima 0.2.4: *rfMaxima* is an RF toolbox for the *wxMaxima* computer algebra system. *rfMaxima* allows for symbolic derivation, as well as numerical evaluation (incl. Bode and Smith chart plotting), of 2-port network (ABCD, G, InverseABCD, H, S, Y, and Z), noise and stability parameters. Derivations are based on the solution of the set of Kirchoff current and voltage law equations representing the 2-port. Expressions can be exported to HTML or TeX. Figures can be exported to EPS or PNG. http://rfmaxima.sourceforge.net
- Verilog-A Large-Signal RF MEMS Model Library: The Verilog-A models can be used with SPICE solvers for DC, small-signal (AC, S-parameters) and large-signal (HB, PSS, QPSS) simulation of analog/RF circuits based on RF MEMS components (capacitors, resonators, switches, varactors). http://rfmems.sourceforge.net

Near-Field to Far-Field Transformation for Antenna Measurements (NF2FF) - Mozilla Firefox

File Edit View History Bookmarks Tools Help

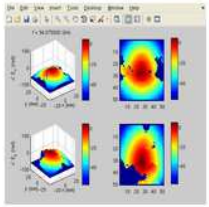
Near-Field to Far-Field Transf...

nf2ff.sourceforge.net

Wikipedia (en)

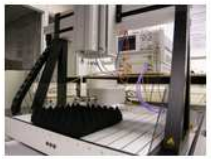
Near-Field to Far-Field Transformation for Antenna Measurements (NF2FF)

DOCUMENTATION DOWNLOAD SCREENSHOTS SUPPORT



Near field (NF) ranges offer a convenient alternative to compact antenna test ranges (CATR) and anechoic far field ranges for the measurement of phased arrays [1,2,3,4,5,6,7,8,9]. NF sites allow for hologram analysis, low sidelobes characterization, and do not require a rotating pedestal capable of bearing the weight of the phased array. The primary objective of the NF2FF sourceforge project is to provide the phased array community with an open-source MATLAB alternative to proprietary NF measurement software. The code features planar near field to far field transforms with rectangular waveguide probe correction. The secondary objective of the project is to implement various functions for phased array hologram analysis. Phased array holograms allow for faulty element localization [5] and for measurement of active element amplitude and phase excitation, in transmit (Tx) as well as in receive (Rx) mode, which allows for insight in the difference between achieved and desired Tx and Rx array factor. In addition, active element Tx and Rx root mean square (RMS) amplitude and phase error can be measured which allows for insight in beam pointing error and side lobe level increase, and gain reduction, while scanning [10].

Hologram analysis can also be used to study near field communication (NFC) antennas.



Assumptions

The script assumes:

- Rectangular coordinate system with z axis normal to planar aperture
- exp(j*omega*t) time dependence convention. Please, substitute i with -j whenever implementing exp(-i*omega*t) time dependence convention based algorithms.

Datasets

Figure 2: nf2ff.sourceforge.net

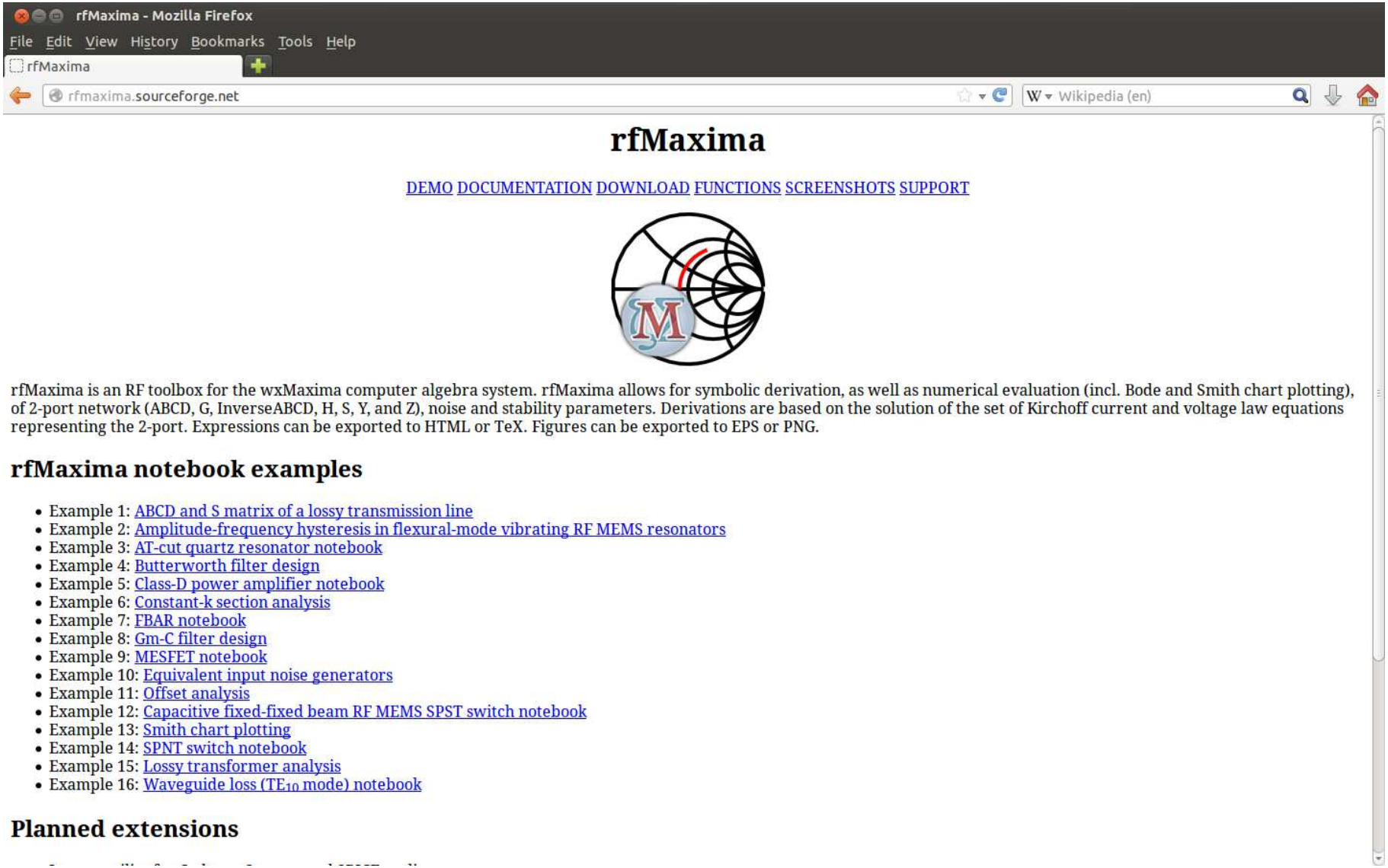


Figure 3: rfmaxima.sourceforge.net

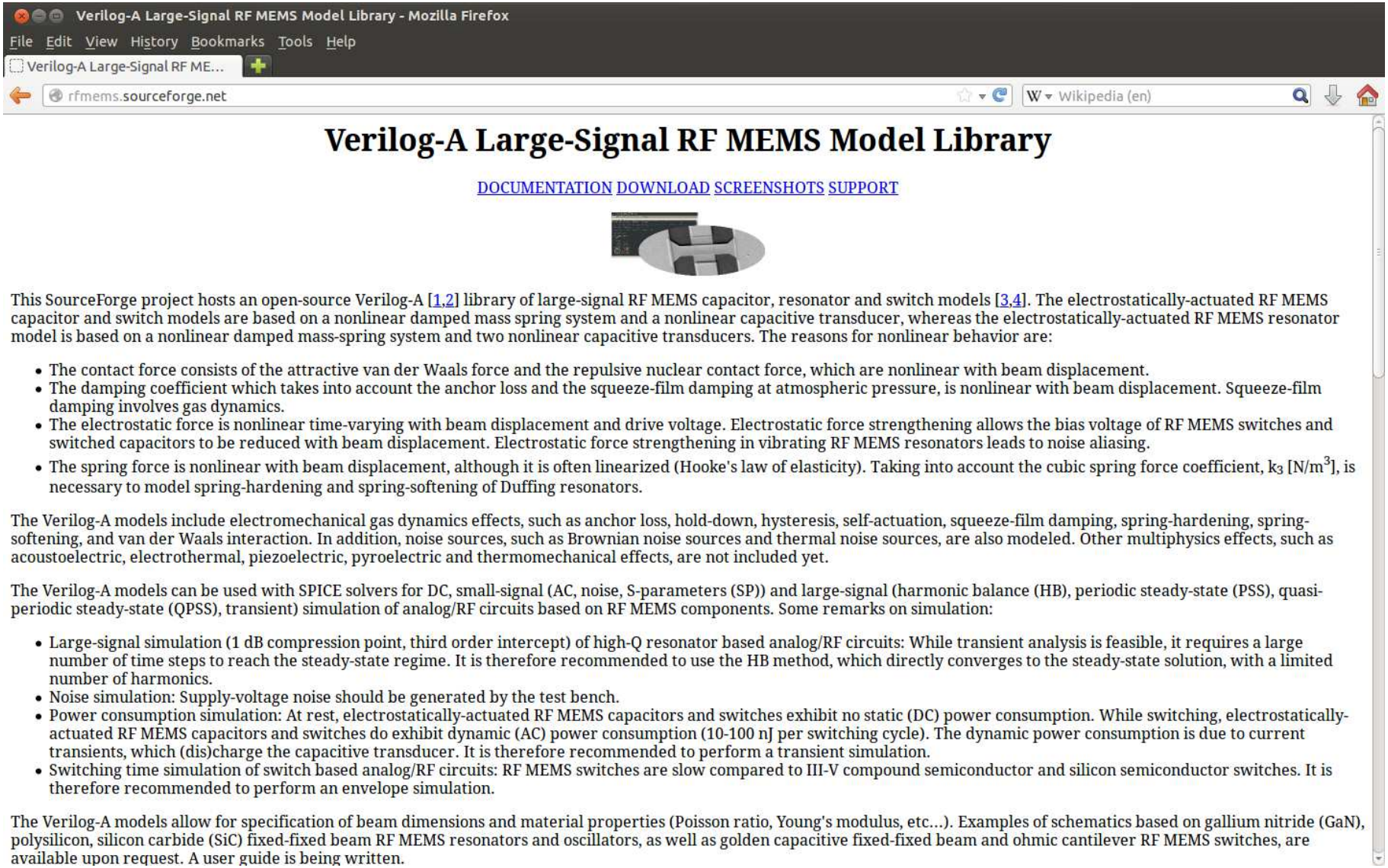


Figure 4: rfmems.sourceforge.net

How to install the 1-DOF Verilog-A compact models:

- Agilent ADS:
  - Copy the files with *ael* extension into the *networks* subdirectory of the ADS project.
  - If necessary, make a *veriloga* subdirectory in the ADS project.
  - Copy the files with *va* extension into the *veriloga* subdirectory of the ADS project.
  - Close and reopen the ADS project.
  - Create a new design.
  - Insert a random component and swap it with FIXED_FIXED_BEAM_RF_MEMS_RESONATOR or FREE_FREE_BEAM_RF_MEMS_RESONATOR.
- Cadence Virtuoso Schematic Editor:
  - *CIW*: *File* → *New* → *Cellview*...
  - *Create New File*: Cell Name: FIXED_FIXED_BEAM_RF_MEMS_RESONATOR or FREE_FREE_BEAM_RF_MEMS_RESONATOR, View Name: *veriloga*, Tool: *VerilogA-Editor*. Click "OK".
  - The editor will appear. Copy/paste the Verilog-A code into the editor. Save it and exit the editor.
  - A dialog box will appear and ask you if you want to create a new symbol. Click "Yes".
  - The *Symbol Generation Options* window will appear. Make appropriate changes and click "OK".
  - Create a new schematic and insert an instance of the FIXED_FIXED_BEAM_RF_MEMS_RESONATOR component or the FREE_FREE_BEAM_RF_MEMS_RESONATOR component.

Acronyms

2G/3G/4G	second generation/third generation/fourth generation
ACLR	adjacent channel leakage ratio
ADC	analog to digital converter
AESA	active electronically scanned array
AMS	analog-mixed signal
AMT	antenna matching tuner
ASM	antenna switch module
BAW	bulk acoustic wave
BEOL	back end of line
BT	bluetooth
BTO	barium titanate
CA	carrier aggregation
CMOS	complementary metal oxide semiconductor
CPU	central processing unit
CRF	coupled resonator filter
CSD	chemical solution deposition
DDS	direct digital synthesizer
DMS	dual mode SAW
DPX	duplexer
DSP	digital signal processor
EMI	electromagnetic interference
EVM	error vector magnitude
ET	envelope tracking
FBAR	film bulk acoustic resonator
FDD	frequency division duplex
FD-SOI	fully-depleted silicon-on-insulator
FEA	finite element analysis
FEM	front-end module
GPU	graphical processing unit
GSM	global system for mobile communications
HB	harmonic balance
HBT	heterojunction bipolar transistor
HDL	hardware description language
HETNET	heterogeneous network
IC	integrated circuit
IEEE	institute for electrical and electronics engineers
IL	insertion loss
IP	intellectual property
MBE	molecular beam epitaxy
MEMS	micro electromechanical system
MIMO	multiple-in multiple-out
MOCVD	metallo-organic chemical vapor deposition
MMMB	multi mode multi band
LNA	low noise amplifier
LTE	long term evolution
LTE-A	long term evolution - advanced
PA	power amplifiers
PAE	power added efficiency
PCM	process control monitor
PDK	process development kit
PD-SOI	partially-depleted silicon-on-insulator
PESA	passive electronically scanned array
PMIC	power management integrated circuit
PLD	pulsed laser deposition
PSS	periodic steady state
PVT	process voltage temperature
PZT	lead zirconate titanate
Q	quality factor
QFN	quad-flat no-leads
QPSS	quasi-periodic steady-state
QS	quasi-static
RF	radio frequency
RF IC	radio frequency integrated circuit
RSSI	received signal strength indicator
RX	receiver
SAR	specific absorption rate
SAW	surface acoustic wave
SKU	stock keeping unit
SMR	solidly mounted resonator
SMT	surface mount technology
SNR	signal to noise ratio
SoC	system-on-chip
SPNT	single pole N throw
TDD	time division duplex
TX	transmitter
UMTS	universal mobile telecommunication system
VSWR	voltage standing wave ratio
WLAN	wireless local area network
WLCSP	wafer level chip scale package
WPAN	wireless personal area network